

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
4 August 2005 (04.08.2005)

PCT

(10) International Publication Number
WO 2005/071426 A1

(51) International Patent Classification⁷: **G01R 31/3185**

(21) International Application Number:
PCT/IB2005/050152

(22) International Filing Date: 13 January 2005 (13.01.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
04100143.9 19 January 2004 (19.01.2004) EP

(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **DINGEMANSE, Johannes, D.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agents: **ELEVELD, Koop, J.** et al.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

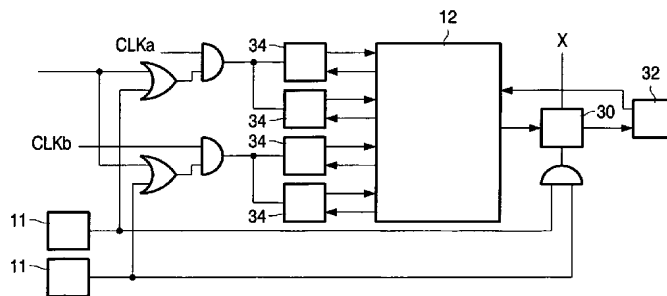
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE,

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(54) Title: TESTING OF CIRCUITS WITH MULTIPLE CLOCK DOMAINS



(57) Abstract: A circuit under test (24) has a scan chain comprising flip-flop cells (IOa-c) with inputs and outputs operationally connected to the logic circuits (12). Different clock domains each contain a respective part of the flip-flop cells (IOa-c) that are clocked by a respective domain clock signal (CLKa, CLKb, CLKc). A set of test input patterns is selected, each with an associated combination of domain clock signals that will be selectively enabled to capture a response to the test pattern. The set contains particular test patterns that have the properties that (a) the response captured by a timing sensitive flip-flop cell (1 Oa-c) in a first clock domain is used to detect a fault, (b) the timing sensitive flip-flop cell (IOa-c) receives data dependent on data from a source flip-flop cell (IOa-c) that belongs to a second clock domain different from the first clock domain, and (c) the combination of selectively enabled domain clock signals associated with the particular test pattern comprises the clocks of both the first and second domain. These particular test patterns also have the property that the data value in the source flip-flop cell (1 Oa-c) is identical to a response value captured by the source flip-flop cell (10a-c) for the particular test pattern. Preferably, the set of test patterns is generated for a virtual circuit obtained by additional logic circuits (30, 40, 42) are added to the design of real the circuit under test. The additional logic circuits (30, 40, 42) are designed to selectively enable a dependence of an input signal of the timing sensitive flip-flop cell (1 Oa-c) on data from the source flip-flop cell (1 Oa-c) when the input and output signals of the source flip-flop cell (10a-c) are identical and the second domain clock is enabled.



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Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

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